CLAIMS

1. (Cancelled)

2. (Currently Amended) The invention as recited in claim [[1]] 11, wherein the second voltage V_{int} is

$$V_{int} = (I_{icp}\Delta t/C1),$$

where I_{icp} is a current of the integral charge pump set by the up/down signal, Δt is a time interval based on the sampling rate of the data, and $C1$ is the capacitance of the capacitor.

3. (Original) The invention as recited in claim 2, wherein the first voltage V_{prop} is

$$V_{prop} = I_{pcp} * R1,$$

where I_{pcp} is a current of the proportional charge pump set by the up/down signal, and $R1$ is a resistance of a resistor across which the first voltage appears.

4. (Original) The invention as recited in claim 3, wherein a stability ζ of the PLL is:

$$\zeta \propto \frac{V_{prop}}{V_{\text{int}}} = \frac{I_{pcp}}{I_{icp}\Delta t} R1C1 .$$

5. (Currently Amended) ~~The invention as recited in claim 1,~~ A phase-locked loop (PLL) comprising:

a phase detector (PD) adapted to generate an up/down signal based on a phase difference between a data signal and a clock signal input to the PD, wherein the phase error is generated by sampling of the clock signal by the data signal;

a proportional charge pump adapted to generate a first voltage for a first time period based on the up/down signal;

an integral charge pump adapted to generate a second voltage for a second time period across a capacitor based upon the capacitance of the capacitor, a truncated version of the up/down signal, and a sampling rate of the data by the PD, wherein the second time period is less than the first time period; and

a voltage-controlled oscillator (VCO) adapted to generate the clock signal based upon a combination of the first and second voltages;

wherein the phase detector is a bang-bang phase detector.

6. (Currently Amended) ~~The invention as recited in claim 1,~~ A phase-locked loop (PLL)

comprising:

a phase detector (PD) adapted to generate an up/down signal based on a phase difference between a data signal and a clock signal input to the PD, wherein the phase error is generated by sampling of the clock signal by the data signal;

a proportional charge pump adapted to generate a first voltage for a first time period based on the up/down signal;

an integral charge pump adapted to generate a second voltage for a second time period across a capacitor based upon the capacitance of the capacitor, a truncated version of the up/down signal, and a sampling rate of the data by the PD, wherein the second time period is less than the first time period; and

a voltage-controlled oscillator (VCO) adapted to generate the clock signal based upon a combination of the first and second voltages;

wherein the VCO comprises an inductor-capacitor (LC) oscillator, the combination of the first and second voltages setting a first portion of the LC oscillator capacitance, and a third voltage setting a second portion of the LC oscillator capacitance.

7. (Original) The invention as recited in claim 6, wherein the VCO comprises first and second pairs of varactors, the combination of the first and second voltages setting the first portion of the LC oscillator capacitance of the first pair of varactors, and a third voltage setting second portion of the LC oscillator capacitance of the second pair of varactors.

8. (Original) The invention as recited in claim 6, wherein the third voltage is generated as a combination of the second voltage and a reference voltage.

9. (Original) The invention as recited in claim 8, comprising a temperature compensation circuit having first and second input ports coupled to the second voltage and the reference voltage, respectively, wherein:

the temperature compensation circuit is adapted to generate the third voltage based on a difference between the second voltage and the reference voltage, and

the third voltage tends to operate the VCO in a manner so as to compensate for temperature variations.

10. (Original) The invention as recited in claim 9, wherein the temperature compensation circuit comprises an amplifier having the first and second input ports and an output port coupled to one terminal of a second capacitor, the other terminal of the capacitor coupled to a common voltage and the

third voltage appearing across the second capacitor.

11. (Currently Amended) ~~The invention as recited in claim 1,~~ A phase-locked loop (PLL) comprising:

a phase detector (PD) adapted to generate an up/down signal based on a phase difference between a data signal and a clock signal input to the PD, wherein the phase error is generated by sampling of the clock signal by the data signal;

a proportional charge pump adapted to generate a first voltage for a first time period based on the up/down signal;

an integral charge pump adapted to generate a second voltage for a second time period across a capacitor based upon the capacitance of the capacitor, a truncated version of the up/down signal, and a sampling rate of the data by the PD, wherein the second time period is less than the first time period; and

a voltage-controlled oscillator (VCO) adapted to generate the clock signal based upon a combination of the first and second voltages;

wherein the integral charge pump comprises a return-to-zero charge pump.

12. (Currently Amended) ~~The invention as recited in claim 1,~~ A phase-locked loop (PLL) comprising:

a phase detector (PD) adapted to generate an up/down signal based on a phase difference between a data signal and a clock signal input to the PD, wherein the phase error is generated by sampling of the clock signal by the data signal;

a proportional charge pump adapted to generate a first voltage for a first time period based on the up/down signal;

an integral charge pump adapted to generate a second voltage for a second time period across a capacitor based upon the capacitance of the capacitor, a truncated version of the up/down signal, and a sampling rate of the data by the PD, wherein the second time period is less than the first time period; and

a voltage-controlled oscillator (VCO) adapted to generate the clock signal based upon a combination of the first and second voltages;

wherein the proportional charge pump comprises a non-return-to-zero charge pump.

13. (Currently Amended) ~~The invention as recited in claim 1,~~ A phase-locked loop (PLL) comprising:

a phase detector (PD) adapted to generate an up/down signal based on a phase difference between

a data signal and a clock signal input to the PD, wherein the phase error is generated by sampling of the clock signal by the data signal;

a proportional charge pump adapted to generate a first voltage for a first time period based on the up/down signal;

an integral charge pump adapted to generate a second voltage for a second time period across a capacitor based upon the capacitance of the capacitor, a truncated version of the up/down signal, and a sampling rate of the data by the PD, wherein the second time period is less than the first time period; and

a voltage-controlled oscillator (VCO) adapted to generate the clock signal based upon a combination of the first and second voltages;

further comprising a phase-frequency detector and a multiplexer (MUX), wherein:

the frequency-phase detector is adapted to:

1) compare the clock signal and a reference signal,

2) generate a switch signal based on the comparison of the clock signal and the reference signal, and

3) generate a phase difference between the clock signal and the reference signal; and

the MUX is adapted to select either i) the up/down signal or ii) the phase difference between the clock signal and the reference signal as an input to the proportional and integral charge pumps,

wherein the proportional and integral charge pumps generate the first and second voltages based upon the phase difference between the clock signal and the reference signal when selected as the input by the MUX.

14. (Currently Amended) The invention as recited in claim [[1]] 11, further comprising a divide-by-N, N a positive number, the divide-by-N adapted to divide an output signal of the VCO by N to provide the clock signal.

15. (Currently Amended) The invention as recited in claim [[1]] 11, wherein the PD is further adapted to generate a retimed data signal based on the clock signal, wherein the retimed data signal is generated by the PD by sampling of the data signal by the clock signal.

16. (Currently Amended) The invention as recited in claim [[I]] 11, wherein the PLL is embodied in an integrated circuit.

17. (Canceled)

18. (Currently Amended) The invention as recited in claim [[17]] 21, wherein, for step (c), the second voltage V_{int} is

$$V_{int} = (I_{icp}\Delta t/C1),$$

where I_{icp} is a current of the integral charge pump set by the up/down signal, Δt is a time interval based on the sampling rate of the data, and $C1$ is the capacitance of the capacitor.

19. (Original) The invention as recited in claim 18, wherein, for step (c), the first voltage V_{prop} is

$$V_{prop} = I_{pcp} * R1,$$

where I_{pcp} is a current of the proportional charge pump set by the up/down signal, and $R1$ is a resistance of a resistor across which the first voltage appears.

20. (Original) The invention as recited in claim 19, wherein a stability ζ of the PLL is:

$$\zeta \propto \frac{V_{prop}}{V_{\text{int}}} = \frac{I_{pcp}}{I_{icp}\Delta t} R1C1 .$$

21. (Currently Amended) ~~The invention as recited in claim 17,~~ A method of implementing a phase-locked loop (PLL) comprising the steps of:

(a) generating, by a phase detector (PD), an up/down signal based on a phase difference between a data signal and a clock signal input to the PD, wherein the phase error is generated by sampling of the clock signal by the data signal;

(b) generating a first voltage for a first time period based on the up/down signal; and

(c) generating a second voltage for a second time period across a capacitor based upon the capacitance of the capacitor, a truncated version of the up/down signal, and a sampling rate of the data by the PD, wherein the second time period id less than the first time period;

(d) combining the first and second voltages; and

(e) generating, with a voltage-controlled oscillator (VCO), the clock signal based upon the combination of the first and second voltages;

wherein, for step (a), the phase detector is a bang-bang phase detector.

22. (Currently Amended) ~~The invention as recited in claim 17,~~ A method of implementing a phase-locked loop (PLL) comprising the steps of:

(a) generating, by a phase detector (PD), an up/down signal based on a phase difference between a data signal and a clock signal input to the PD, wherein the phase error is generated by sampling of the clock signal by the data signal;

(b) generating a first voltage for a first time period based on the up/down signal; and

(c) generating a second voltage for a second time period across a capacitor based upon the capacitance of the capacitor, a truncated version of the up/down signal, and a sampling rate of the data by the PD, wherein the second time period id less than the first time period;

(d) combining the first and second voltages; and

(e) generating, with a voltage-controlled oscillator (VCO), the clock signal based upon the combination of the first and second voltages;

wherein, for step (e), the VCO comprises an inductor-capacitor (LC) oscillator, and step (d) comprises the steps of (d1) setting a first portion of the LC oscillator capacitance based on the combination of the first and second voltages, (d2) generating a third voltage, and (d3) setting a second portion of the LC oscillator capacitance based on the third voltage.

23. (Original) The invention as recited in claim 22, wherein, for step (e), the VCO comprises first and second pairs of varactors, the combination of the first and second voltages setting the first portion of the LC oscillator capacitance of the first pair of varactors, and the third voltage setting second portion of the LC oscillator capacitance of the second pair of varactors.

24. (Original) The invention as recited in claim 22, wherein the third voltage is generated by the step of combining the second voltage and a reference voltage.

25. (Original) The invention as recited in claim 24, comprising the steps of:

generating the third voltage based on a difference between the second voltage and the reference voltage, and

operating, based on the third voltage, the VCO in a manner so as to compensate for temperature variations.

26. (Currently Amended) ~~The invention as recited in claim 17~~, A method of implementing a phase-locked loop (PLL) comprising the steps of:

(a) generating, by a phase detector (PD), an up/down signal based on a phase difference between a data signal and a clock signal input to the PD, wherein the phase error is generated by sampling of the clock signal by the data signal;

(b) generating a first voltage for a first time period based on the up/down signal; and

(c) generating a second voltage for a second time period across a capacitor based upon the capacitance of the capacitor, a truncated version of the up/down signal, and a sampling rate of the data by the PD, wherein the second time period id less than the first time period;

(d) combining the first and second voltages; and

(e) generating, with a voltage-controlled oscillator (VCO), the clock signal based upon the combination of the first and second voltages;

further comprising the steps of:

comparing the clock signal and a reference signal,

generating a switch signal based on the comparison of the clock signal and the reference signal, and

generating a phase difference between the clock signal and the reference signal; and

selecting either i) the up/down signal or ii) the phase difference between the clock signal and the reference signal as an input to the proportional and integral charge pumps, and

wherein the first and second voltages are generated based upon the phase difference between the clock signal and the reference signal when selected as the input by the MUX.

27. (Currently Amended) The invention as recited in claim [[17]] 21, further comprising the step of generating a retimed data signal based on the clock signal, wherein the retimed data signal is generated by the PD by sampling of the data signal by the clock signal.

28. (Currently Amended) The invention as recited in claim [[17]] 21, wherein the method is embodied as steps of a processor in an integrated circuit.

29. (New) The invention as recited in claim 11, wherein the phase detector is a bang-bang phase detector.

30. (New) The invention as recited in claim 11, wherein the VCO comprises an inductor-capacitor (LC) oscillator, the combination of the first and second voltages setting a first portion of the LC oscillator capacitance, and a third voltage setting a second portion of the LC oscillator capacitance.

31. (New) The invention as recited in claim 11, further comprising a phase-frequency detector and a multiplexer (MUX), wherein:

the frequency-phase detector is adapted to:

1) compare the clock signal and a reference signal,

2) generate a switch signal based on the comparison of the clock signal and the reference signal, and

3) generate a phase difference between the clock signal and the reference signal; and

the MUX is adapted to select either i) the up/down signal or ii) the phase difference between the clock signal and the reference signal as an input to the proportional and integral charge pumps,

wherein the proportional and integral charge pumps generate the first and second voltages based upon the phase difference between the clock signal and the reference signal when selected as the input by the MUX.

32. (New) The invention as recited in claim 12, wherein the phase detector is a bang-bang phase detector.

33. (New) The invention as recited in claim 12, wherein the VCO comprises an inductor-capacitor (LC) oscillator, the combination of the first and second voltages setting a first portion of the LC oscillator capacitance, and a third voltage setting a second portion of the LC oscillator capacitance.

34. (New) The invention as recited in claim 12, further comprising a phase-frequency detector and a multiplexer (MUX), wherein:

the frequency-phase detector is adapted to:

1) compare the clock signal and a reference signal,

2) generate a switch signal based on the comparison of the clock signal and the reference signal, and

3) generate a phase difference between the clock signal and the reference signal; and

the MUX is adapted to select either i) the up/down signal or ii) the phase difference between the clock signal and the reference signal as an input to the proportional and integral charge pumps,

wherein the proportional and integral charge pumps generate the first and second voltages based upon the phase difference between the clock signal and the reference signal when selected as the input by the MUX.